CLAIMS

1. A method for generating test patterns for testing a register transfer level digital circuit, the method comprising:

generating an assignment decision diagram of the register transfer level digital circuit;

identifying modules in the assignment decision diagram;

determining objectives for the identified modules using a nine-valued symbolic algebra;

justifying and propagating the objectives by traversing the assignment decision diagram to obtain a test environment; and

applying predetermined test vectors through the register transfer level digital circuit using the test environment obtained.

2. The method of claim 1 wherein generating of the assignment decision diagram comprises receiving a hardware description language representation of the register transfer level digital circuit and converting the hardware description language representation of the register transfer level digital circuit into the assignment decision diagram.

3. The method of claim 1 wherein the assignment decision diagram comprises a graph-like structure representing functional behavior of the register transfer level digital circuit and an approximate structural representation of the register transfer level digital circuit.

4. The method of claim 1 wherein the identified modules comprise arithmetic operations, logic arrays, random logic blocks, storage elements, interconnects and black boxes.

5. The method of claim 1 wherein the objectives comprises symbolic variables representing values at inputs and outputs of the register transfer level digital circuit and the identified module and a frame cycle.

6. The method of claim 5 wherein the objectives further comprises symbolic variables representing values at inputs and outputs of the register transfer level digital circuit and the identified module, a frame cycle and a state.

7. The method of claim 1 wherein the algebra comprises symbolic variables representing the ability of a value to be controlled to one of a value and a state.

8. The method of claim 7 wherein the algebra comprises symbolic variables representing the ability of a value to be observed.

9. The method of claim 1 wherein the algebra comprises symbolic variables comprising controllability to one, controllability to zero, controllability to all ones, controllability to a constant, controllability to a state, controllability to an arbitrary value, controllability to a high impedance state, observeability of a fault, and complement observeablity of a fault.

10. The method of claim 1 wherein justifying and propagating objectives comprises justifying test vectors to inputs of the identified modules from primary inputs of the digital circuit and propagating test responses from the outputs of the identified modules to primary outputs of the register transfer level digital circuit.

11. The method of claim 1 wherein justifying and propagating objectives comprises a branch and bound search procedure having a backtracking and a time limit.

12. The method of claim 1 wherein the test environment comprises a set of justification and propagation paths from primary inputs to primary outputs of the identified modules which exercises the module when test vectors are applied at the primary inputs.

13. The method of claim 12 wherein the justification and propagation paths span many clock cycles.

14. The method of claim 1 further comprising utilizing heuristics to obtain the test environment.

15. The method of claim 1 further comprising continuing to identify modules, determine objectives, justify and propagate objectives and apply predetermined test vectors for each of the modules identified and for each test environment obtained to obtain system-level test sets for each of the module identified.

16. The method of claim 15 further comprising concatenating system-level test sets for each of the modules identified to obtain a complete test set for the register transfer level digital circuit.

17. The method of claim 15 wherein the test vectors are obtained from a test set library.

18. A method of generating test patterns for testing a register transfer level digital circuit, the method comprising:

receiving a functional register transfer level circuit design of the digital circuit having a single clock line;

generating a data structure from the circuit design received;

identifying logic structures and blocks from the data structure generated;

justifying test objectives from inputs of the logic structures and blocks to primary inputs of the register transfer level digital circuit to identify justification paths;

propagating test objectives from outputs of the logic structures and blocks to primary outputs of the register transfer level digital circuit to identify propagation paths; and

applying predetermined test vectors through the digital circuit using the justification and propagation paths identified.

19. The method of claim 18 wherein generating the data structure comprises representing the register transfer level circuit design using a hardware description language representation and converting the hardware description language representation into an assignment decision diagram.

20. The method of claim 19 wherein the assignment decision diagram comprises a graph-like structure representing functional behavior of the register transfer level digital circuit and an approximate structural representation of the register transfer level digital circuit.

21. The method of claim 18 wherein the identified logic structures and blocks comprise arithmetic operations, logic arrays, random logic blocks, storage elements, interconnects and black boxes.

22. The method of claim 18 wherein justifying test objectives and propagating test objectives comprises using objectives determined by a nine-valued algebra.

23. The method of claim 22 wherein the objectives comprises symbolic variables representing values at inputs and outputs of the register transfer level digital circuit and the identified logic structures and blocks and a frame cycle.

24. The method of claim 22 wherein the objectives further comprises symbolic variables representing values at inputs and outputs of the register transfer level digital circuit and the identified logic structures and blocks, a frame cycle and a state.

25. The method of claim 22 wherein the algebra comprises symbolic variables representing the ability of a value to be controlled to one of a value and a state.

26. The method of claim 25 wherein the algebra comprises symbolic variables representing the ability of a value to be observed.

27. The method of claim 22 wherein the algebra comprises nine symbolic variables comprising controllability to one, controllability to zero, controllability to all ones, controllability to a constant, controllability to a state, controllability to an arbitrary value, controllability to a high impedance state, observeability of a fault, and complement observeablity of a fault.

28. The method of claim 18 further comprising utilizing heuristics to identify justification and propagation paths.

29. The method of claim 18 further comprising continuing to identify logic structures and blocks, justify test objectives, propagate test objectives and apply predetermined test vectors for each of the logic structures and blocks identified for each of the justification and propagation paths identified to obtain system-level tests set for each of the logic structures and blocks identified.

30. The method of claim 29 further comprising concatenating system-level test sets for each of the logic structures and blocks identified to obtain a complete test set for the register transfer level digital circuit.

31. The method of claim 1 wherein the test vectors are obtained from a test set library.